VLIW COMPUTER PROCESSING ARCHITECTURE HAVING A SCALABLE NUMBER OF REGISTER FILES

ABSTRACT OF THE DISCLOSURE

According to the invention, a processing core (12) comprising one or more processing pipelines (100) having N-number of processing paths (56), each of which process instructions (54) on M-bit data words. In addition, the processing core (12) includes a plurality of register files (60), each preferably having Q-number of registers which are M-bits wide. Preferably, every two of the processing paths (56) share one register file (60). A processing instruction (52) preferably comprises N-number of P-bit instructions (54) appended together to form a very long instruction word (VLIW), and the N-number of processing paths (56) preferably process the N-number of P-bit instructions (54) in parallel. In accordance with one preferred embodiment of the invention, M is 64, Q is 64 and P is 32. Accordingly, the N-number of processing paths (56), each process 32-bit instructions (54) on 64-bit data words, and the plurality of register files (60) each have 64 registers which are 64-bits wide. Processing pipeline (100) preferably comprises a fetch stage (110), a decode stage (120), an execute stage (130) and a write-back stage (140). The execute stage (130) preferably comprises an execute unit (134) for each of the N-number of processing paths (56). Each execute unit (134) includes an integer processing unit (64), a load/store processing unit (66), a floating point processing unit (68), or any combination of one or more of those units. Unlike prior art processor designs, an integer processing unit (64) and a floating point processing unit (68) in one or more of the execute units (134) share a single register file (60).